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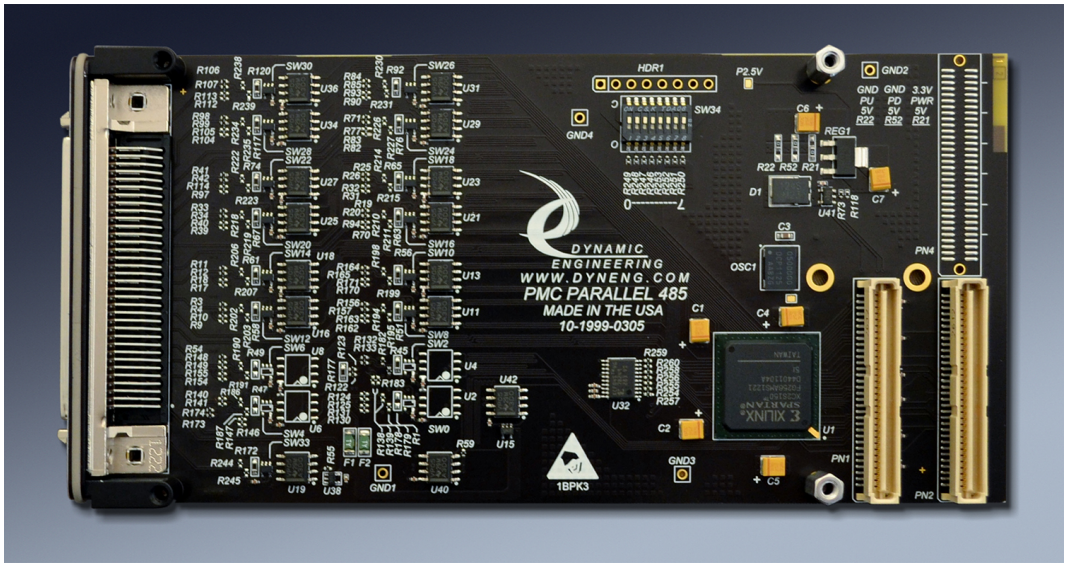
User Manual

PMC-PARALLEL-485-NG1

RS485 Parallel Interface
PMC Module



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PMC-PARALLEL-485-NG1

RS485 Parallel Interface
PMC Module

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This product has been designed to operate with PMC Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Revised 12/27/22

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Product Description

PMC-PARALLEL-485 is part of the PCI Mezzanine Card [PMC] family of modular I/O components. PMC-PARALLEL-485 provides 32 differential IO in one PMC position. The IO are brought to a 68 pin SCSI 3 style connector and/or the backplane connector. In addition, a bi-directional clock and clock enable differential pair are provided at the front panel.

Each of the 32 differential pairs is programmable to be an input or an output. The lower 4 bits [0-3] are individually programmable. The remaining bits are programmed on a nibble basis. Input, Output, Termination active or disabled.

The IO remaining after special functions are available as inputs in two forms. The data can be read directly without filtering and from a data latch which captures any detected 'hi' condition. The data can be selectively inverted and masked prior to the latch function. The direct read data is unaffected by the inversion and masking. The output lines are directly driven from a register.

The 485 transceivers are selectively enabled for transmitting and always enabled for receiving. Separate input and output lines between the FPGA and the transceivers allow for local loop-back if the transceivers are enabled to transmit.

Each differential pair has a 100Ω parallel termination resistor. Analog switches are programmed to activate the termination when the termination bit for an IO pair is set. The resistance stated includes the analog switch contribution. For cable terminated environments the analog switches and resistors can be programmed to be disabled.

Eight “user bits” are supplied for user configuration control.

PMC-PARALLEL-485 conforms to the PMC standard. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

The NG1 version features:

Two clock generators are provided. Each generator can be referenced to either the external source, the local oscillator [50 MHz converted to 2 MHz] or the PCI/2 clock. The generators are programmable [12 bits].

The generated frequencies are then used as the reference for two counters. One counter is 32 bits wide and the other is 14. The output of the counters is available via the PCI bus. The output of the 32 bit counter is captured based on the state of the 14 bit counter and available from a second register.

All configuration registers support read and write operations for maximum software convenience. LW operations are supported (please refer to the memory map).

IO_0 has fuse protected 3.3V power connected. Fuses are rated at 100 mA per side.

IO1, IO_2 are tied to ground.

In addition IO3 is received [Reset In] and redriven to IO4 and IO5 [Reset Out] with IO6 providing an optional second source.

180 ohm resistors are installed in place of standard 100 ohm parallel terminations.

“P” side pull-ups are installed – 2.2K ohms to 5V on IO_12 - IO_23.

Bezel and Pn4 IO implemented.

Theory of Operation

PMC-PARALLEL-485 is a part of the PMC family of modular I/O products. It meets the PMC Module Standard. It is assumed that the reader is at least casually familiar with this document and logic design.

PMC-PARALLEL-485 is designed for the purpose of transferring data from one point to another with a parallel protocol. PMC-PARALLEL-485 features a Xilinx FPGA and 34 differential transceivers. The transceivers can be programmed to be drivers or receivers. Terminations can be programmed to be active or disabled. Controls are individual for the bits 0-3 and by groups of four IO for IO 4-31. The clock and clock enable have a common direction control. The FPGA contains the PCI interface and control required for the parallel interface.

The PCI interface is achieved with the Dynamic Engineering PCI Core design. The PCI Core design handles the decoding of the PCI bus, responding to Configuration and Target access types for this design. 64K of memory is requested in this application.

Three registers are used to interact with the basic data interface. The output data register [pmc_par485_dataout] is connected to the driver side of the ‘485 transceiver. The input register [pmc_par485_datain] is readable from the host and is connected to the receive side of the transceiver. The direction register [pmc_par485_dir_term] has a bit corresponding to each IO or nibble group controling the direction of each transceiver. The direction controls default to read. The terminations are programmed through the same register. If set to drive the bus the value driven corresponds to the bit in the output data register. The output data register is read-writeable and because the register is independent of the bus, the data read will always match the data written allowing read-modify-write operations. The separate input register provides access to the IO bus side of the drivers. The data read will reflect the state of the bus and not necessarily the state of the on-board drivers.

With the -NG1 version of the design, care must be used to account for the various unusual features which over-ride some of the IO lines. Please see the connector definitions and register descriptions for more detail.

Input data is registered and clocked with the PCI bus clock. The data is available "as-is" via the "datain" register. A filtered version of the data is available from the "datain_lat" register. Each data input line has two corresponding filter control bits in the "pol" and "mask" registers. The "pol" register controls inversion of the input

data. The "mask" register controls which bits can be latched by the data latch. Once a filtered data bit is captured the data is held in the latch until read. Once read the latch is cleared until new data is detected. The latch is not an edge detector. If the mask is on and the inversion is off and the signal is a level the bit will be set as soon as the reset has completed after the read. Known level state bits should, most likely, be masked off or inverted to detect unusual or error situations.

The -NG1 version of the PMC_Parallel_485 has two added features. A 32 bit counter and a 14 bit counter each with separate clock generators. The clock generators can utilize an external clock, the PCI clock divided by 2, or the onboard reference oscillator [50 MHz divided down to 2 MHz.]. The generator can be programmed to further divide the reference down to a user selected frequency. The "clk1" and "clk2" registers control the operation of the generators.

The Counter bit at the selected [mux'd] counter output is used to create a one clock wide pulse referenced to the 32 bit counter. The pulse is used to selectively capture the 32 bit count at that time. The captured count will remain in the register until over-written by the next edge_detected write. The period is a function of the reference rate for the 14 bit counter and the bit which is selected to control the capture function. It is **assumed** that the clock rate of the 32 bit counter is faster than the rate of the 14 bit counter bit selected. At least a 4:1 margin is desired to allow the capture process to happen properly. The lowest reference bit from the 14 bit counter is (5) which corresponds to divide by 32 so this should not be much of a limitation.

The interrupts available on the -NG1 version correspond to the two rollover conditions and edge detection. The three interrupt sources are sampled and when the signal is de-asserted the corresponding interrupt bit set. The hardware waits for the de-assertion of the signal to make sure that the data is captured in the edge detect mode and that the reset has occurred with the RST bits. With the slower clock rates the interrupt could be processed before the data is captured if the active edge was used to trigger the interrupt event. Each interrupt generator source is individually maskable. The interrupt state is available masked and unmasked in the "intstat" register to allow polling and interrupt priority processing. In addition an extra signal [force int] is supplied to allow software generated interrupts for development and debugging purposes.

Several "special" bits are provided. Of the 32 IO lines one pair (2) are dedicated to providing fused 3.3V power, two pair (4) are dedicated ground references, 3

pair plus one single ended signal are used for a reset circuit [4 IO effectively] plus the 4 pair used to receive or transmit the RST and CLK signals for each of the counters. The net affect is that IO7 and IO12-31 are available for general purpose use. IO0-6, and 8-11 are used for special purposes. Please refer to the connector definitions for the pin definitions.

Address Map

Function	Offset	Function
// PMC relative addresses //		
#define pmc_par485_clk1	0x00	// channel 1 divider control
#define pmc_par485_clk2	0x04	// channel 2 divider control
#define pmc_par485_int	0x08	// interrupt mask register
#define pmc_par485_mask	0x0C	// data in latch mask register
#define pmc_par485_pol	0x10	// data in polarity selection reg.
#define pmc_par485_dir_term	0x14	// direction and termination reg.
#define pmc_par485_dataout	0x18	// output data register
#define pmc_par485_loadcnt1	0x1C	// counter 1 load value register
#define pmc_par485_loadcnt2	0x20	// counter 2 load value register
#define pmc_par485_datain	0x24	// data input register
#define pmc_par485_datain_lat	0x28	// data input latched register
#define pmc_par485_intstat	0x2C	// interrupt status register
#define pmc_par485_rdcnt32	0x30	// 32 bit counter current count reg.
#define pmc_par485_rdedgcnt	0x34	// 32 bit cntr when edge detect
#define pmc_par485_loadcnt32	0x38	// load 32 bit cntr w/ loadcnt1
#define pmc_par485_rdcnt14	0x3C	// 14 bit counter current value
#define pmc_par485_loadcnt14	0x40	// load 14 bit cntr w/ loadcnt2
#define pmc_par485_sw	0x44	// read the user dip switch setting

FIGURE 1 PMC-PARALLEL-485 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within PMC-PARALLEL-485. The addresses are all offsets from a base address. The carrier board, that the PMC is installed into, provides the base address.

Programming

Programming PMC-PARALLEL-485 requires only the ability to read and write data in the host's PMC space. The base address is determined by the PMC Carrier board. This documentation refers to the address of the PMC space, for the slot that the PMC is installed in, as the base address.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

PMC_Parallel_485 has a VendorID of 0x10EE and a CardID of 0x0004. Your driver can use the configuration information to identify the PMC-Parallel-485 during initialization in systems where address spaces are allocated dynamically.

Register Definitions

pmc_par485_clk1

[$00 parallel-485 CLK Control Port read/write]

CONTROL REGISTER CLK1	
DATA BIT	**DESCRIPTION**
31-18	SPARE
17	RESET SOURCE SELECT
16	Reserved set to 0
15	Reserved set to 0
14-13	CLK PRE-SELECTOR
12	CLK POST SELECTOR
11-0	DIVISOR

FIGURE 2 PMC-PARALLEL-485 CLK1 BIT MAP

CLK1 is the 32 bit counter control register.

The PS [pre-selector] bits are used to select from the clock sources.
00 = '0' no clock
01 = Oscillator – 2MHz reference
10 = EXT_CLK - received from differential pair CLK1
11 = PCI/2

Divisor [11-0] are the clock divisor select bits. The clock source is divided by a counter and the select bits pick which clock is used to drive the IO read-back registers. The reference clock for the counter is selected with the CLK Pre-Selector. The output frequency is {reference / [2(n+1)]}. N≥1. The reference oscillator is 2 MHz. in frequency. The counter divides by N+1 due to counting from 0 ->n before rolling over. The output is then divided by 2 to produce a square wave output.

Post Selector when '1' sets clock out to clock divided, when '0' sets clock out to pre-selector reference value.

Please note that the 485 buffers are rated for 40 MHz. With most systems the larger divisors will be used. The smaller divisors are provided for use with external oscillators and the external clock line.

Reset Source Select when '1' selects the external reset source associated with

that channel and when '0' selects the reset based on the counter associated with that channel.

pmc_par485_clk2

[$04 parallel-485 CLK Control Port read/write]

CONTROL REGISTER CLK2

DATA BIT	DESCRIPTION
31-23	SPARE
22-20	Edge Detector Selection
19-18	SPARE
17	RESET SOURCE SELECT
16	Reserved set to 0
15	Reserved set to 0
14-13	CLK PRE-SELECTOR
12	CLK POST SELECTOR
11-0	DIVISOR

FIGURE 3 PMC-PARALLEL-485 CLK2 BIT MAP

CLK2 is in the 14 bit counter control register.

The PS [pre-selector] bits are used to select from the clock sources.
00 = ‘0’ no clock
01 = Oscillator - 2 MHz. reference
10 = EXT_CLK - received from differential pair CLK2
11 = PCI/2

Divisor [11-0] are the clock divisor select bits. The clock source is divided by a counter and the select bits pick which clock is used to drive the IO read-back registers. The reference clock for the counter is selected with the CLK Pre-Selector. The output frequency is {reference / [2(n+1)]}. N≥1. The reference oscillator is 2 MHz. in frequency. The counter divides by N+1 due to counting from 0 ->n before rolling over. The output is then divided by 2 to produce a square wave output.

Post Selector when '1' sets clock out to clock divided, when '0' sets clock out to pre-selector reference value.

Please note that the 485 buffers are rated for 40 MHz. With most systems the larger divisors will be used. The smaller divisors are provided for use with external oscillators and the external clock line.

Reset Source Select when '1' selects the external reset source associated with that channel and when '0' selects the reset based on the counter associated with that channel.

Edge Detection Selection Bits

22..20	Bit of counter14 selected
000	5
001	6
010	7
011	8
100	9
101	10
110	11
111	12

pmc_par485_int

[$08 parallel-485 Control Register Port read/write]

CONTROL REGISTER INT

DATA BIT	DESCRIPTION
16	IO7 Mux CNTL
7	FORCE
4	EN_RST2
2	EN_RST1
0	EN_EDGE

FIGURE 4 PMC-PARALLEL-485 INTERRUPT CNTL BIT MAP

When Force = '1' then the INTA signal is driven onto the PCI Bus port causing and interrupt request. Force is used to support test and software development.

EN_RST1,2 when '1' enable the interrupt on reset1,2 condition. When '0' the interrupts are disabled.

EN_EDGE when '1 enables the edge detector interrupt. The edge detector is the muxed selection of one of the upper bits of the 14 bit counter. When set a pulse is generated to enable a latch to capture the current count on the 32 bit counter. When the count has been latched the interrupt is generated.

When the interrupt status is read the state of the interrupt(s) is available. The RSTx and Edge_Detect interrupts are cleared by writing to the Interrupt Status register. The Force interrupt requires clearing by resetting the request bit in the _int register.

When the IO7 Mux Cntl bit is set the IO7 output bit is controlled by the output data register. When cleared the IO7 output bit is controlled by the Edge Detect circuit. A pulse [32 bit counter period wide] is driven each time the edge detect circuit detects a trigger event. The falling edge of the selected counter14 bit is used to determine the trigger event.

pmc_par485_mask

[$0C parallel-485 Mask Port read/write]

CONTROL REGISTER DIR_TERM	
DATA BIT	**DESCRIPTION**
31-0	1 = enable, 0 = mask off for data input latch

FIGURE 5 PMC-PARALLEL-485 MASK CONTROL BIT MAP

If an input bit is desired to be monitored then the corresponding mask bit should be set to '1'. To keep an input bit from being active set the corresponding bit to '0'.

pmc_par485_pol

[$10 parallel-485 Polarity Port read/write]

CONTROL REGISTER DIR_TERM	
DATA BIT	**DESCRIPTION**
31-0	1 = invert, 0 = normal

FIGURE 6 PMC-PARALLEL-485 POLARITY CONTROL BIT MAP

If an input bit is active low then the corresponding polarity bit should be set to '1'. The data input latch will capture the level of a signal. Active low signals should be inverted to capture the active state.

pmc_par485_dir_term

[$14 parallel-485 direction and termination Port read/write]

CONTROL REGISTER DIR_TERM	
DATA BIT	**DESCRIPTION**
10-0	DIRection 10-0 0 = tristate, 1 = drive
26-16	TERMination 10-0 1 = terminated

FIGURE 7 PMC-PARALLEL-485 CONTROL PORT 1 BIT MAP

The direction for each of the 32 differential pairs is controlled through this port. The port defaults to ‘0’ which corresponds to tri-stating the drivers. The output and input pins are separated and independently connected to the Xilinx to allow loop-back testing. The input side is always active.

Pull-up and Pull-down resistors built into some '485 interface devices may make the signal appear to be driven [if open] when in the tri-stated mode. Enabling the termination on a tristated line will yield approximately 2.5V on each side of the tri-stated driver.

Please note that some of the differential pairs are used for 3.3V, GND, reset, clk and RST signals. IO 12-31 and IO 7 are available for general purpose use. Please see the pinout definitions for more information.

CONTROL	CORRESPONDING IO BIT(S)
DIR_0..3	IO_0..3.
DIR4	IO_4..7
DIR5	IO_8..11
DIR6	IO_12..15
DIR7	IO_16..19
DIR8	IO_20..23
DIR9	IO_24..27
DIR10	IO_28..31

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated and where. In some systems it will make sense to terminate the lines in the cable and in others it will make sense to use the onboard terminations.

CONTROL	CORRESPONDING IO BIT(S)
TERM_0..3	IO_0..3.
TERM4	IO_4..7
TERM5	IO_8..11
TERM6	IO_12..15
TERM7	IO_16..19
TERM8	IO_20..23
TERM9	IO_24..27
TERM10	IO_28..31

pmc_par485_dataout

[$18 parallel-485 Write Port read/write]

CONTROL REGISTER DATA OUT	
DATA BIT	**DESCRIPTION**
31-0	IO31-IO0

FIGURE 8 PMC-PARALLEL-485 DATAOUT BIT MAP

The 32 bits are written through this port. The port is on the single ended side of the transceivers. The data read will match the data written on this port because the FPGA internal register is being read.

pmc_par485_loadcnt1

[$1C parallel-485 read/write]

CONTROL REGISTER Load Count 1	
DATA BIT	**DESCRIPTION**
31-0	32 bit counter pre-load value

FIGURE 9 PMC-PARALLEL-485 CNTR1 PRE-LOAD BIT MAP

The 32 bit counter is pre-loadable. The value to pre-load into the counter is stored in this register

pmc_par485_loadcnt2

[$20 parallel-485 read/write]

CONTROL REGISTER Load Count 2	
DATA BIT	**DESCRIPTION**
31-14	Spare
13-0	14 bit counter pre-load value

FIGURE 10 PMC-PARALLEL-485 CNTR2 PRE-LOAD BIT MAP

The 14 bit counter is pre-loadable. The value to pre-load into the counter is stored in this register

pmc_par485_datain

[$24 parallel-485 data input read only]

Data Input Port	
DATA BIT	**DESCRIPTION**
31-0	value currently on data input lines

FIGURE 11 PMC-PARALLEL-485 DATA IN BIT MAP

The "natural" data from the input port is available on this port. The data input lines are continuously sampled with Xilinx input flip-flops at the PCI clock rate. When a read occurs the value on the flip-flops is returned to the host.

pmc_par485_datain_lat

[$28 parallel-485 data input latch read only]

Latched Data Input Port	
DATA BIT	**DESCRIPTION**
31-0	Spare

FIGURE 12 PMC-PARALLEL-485 DATA IN LATCHED BIT MAP

The filtered and captured input data is available from this port. When read the storage register is cleared. See the Polarity and Mask registers for more details on the filtering capabilities.

pmc_par485_intstat

[$2C parallel-485 interrupt status read/write]

CONTROL REGISTER Interrupt Status

DATA BIT	DESCRIPTION
	Read
31-8	Spare mask off when read
7	Force Int Active
6	Interrupt Request 1 = active
5	RST2 Interrupt masked
4	RST2 Interrupt unmasked
3	RST1 Interrupt masked
2	RST1 Interrupt unmasked
1	Edge Detect Interrupt masked
0	Edge Detect Interrupt unmasked
	Write
4	1 = Clear RST2 Interrupt
2	1 = Clear RST1 Interrupt
0	1 = Clear Edge Detect Interrupt

FIGURE 13 PMC-PARALLEL-485 INTERRUPT STATUS BIT MAP

The interrupt request bits are active high. When the mask is set to '0' then the unmasked requests can be polled without interrupting the host. When set the request stays set until specifically cleared with a write to this address and the corresponding data bit set. The clear is transitory; the bit can be re-activated immediately based on the state of the hardware. The clear can not be used to hold off interrupts. The mask register is for that purpose.

pmc_par485_rdcnt32

[$30 parallel-485 Counter 1 Current State read only]

Counter 1 Current State

DATA BIT	DESCRIPTION
31-0	Current state of the 32 bit counter

FIGURE 14 PMC-PARALLEL-485 CNTR1 CURRENT STATE BIT MAP

A read from this port will provide the current 32 bit count value from Counter 1. The Count is continuously captured and stored into a holding register.

pmc_par485_rdedgcnt

[$34 parallel-485 Counter 1 Edge Detect State read only]

Counter 1 State When Edge Detect was Asserted	
DATA BIT	**DESCRIPTION**
31-0	Current state of the 32 bit counter

FIGURE 15 PMC-PARALLEL-485 CNTR1 CURRENT STATE BIT MAP

A read from this port will provide the current 32 bit count value from Counter 1 when Edge Detect was asserted. The Count is selectively captured and stored into a holding register when Edge Detect is asserted. Value remains in register until overwritten by next Edge Detect capture event.

pmc_par485_ldcnt32

[$38 parallel-485 load Pre-load value write only]

A write to this port will provide load the value stored into the pre-load register for counter 1 into counter 1. The counter is loaded on the next rising edge of the counter reference clock after the load condition is recognised. The load may be delayed up to 1 period of the reference clock and at slow reference rate this can take a while.

pmc_par485_rdcnt14

[$3C parallel-485 Counter 1 Current State read only]

Counter 1 Current State	
DATA BIT	**DESCRIPTION**
13-0	Current state of the 14 bit counter

FIGURE 16 PMC-PARALLEL-485 CNTR2 CURRENT STATE BIT MAP

A read from this port will provide the current 14 bit count value from Counter 2. The Count is continuously captured and stored into a holding register.

pmc_par485_ldcnt14

[$40 parallel-485 load Pre-load value write only]

A write to this port will provide load the value stored into the pre-load register for counter 2 into counter 2. The counter is loaded on the next rising edge of the counter reference clock after the load condition is recognised. The load may be delayed up to 1 period of the reference clock and at slow reference rate this can take a while.

pmc_par485_sw

[$10 Parallel-485 Switch Read Port read only]

CONTROL REGISTER 1	
DATA BIT	**DESCRIPTION**
31-24	Revision Minor
23-16	Revision Major
15-9	Spare
9	CLK_EN_EXT
8	CLK_EXT
7-0	UB7-0

FIGURE 17 PMC-PARALLEL-485 SWITCH READ BIT MAP

The Switch Read Port has the user bits. The user bits are connected to 8 switch positions. The switches allow custom configurations to be defined by the user and for the software to “know” how to configure.

CLK_EXT and CLK_EN_EXT are not used in NG1. The bits are connected to support Acceptance testing of the reset circuit.

Spare bits are set to ‘0’ for this port.

Revision Major, Revision Minor : are set to show the current revision of the FLASH. The Major revision is also refected in the PCI bus revision field. The minor revision is rolled for any change made and the major when something more significant is implemented.

1.0 initial release 1/12/2000
1.1 Switch to DE PCI core, add revision read-back 10/17/16
1.2 Switch to Muxed read-back paths 11/15/22
1.3 Add Force Interrupt feedback in Interrupt Status register 12/27/22

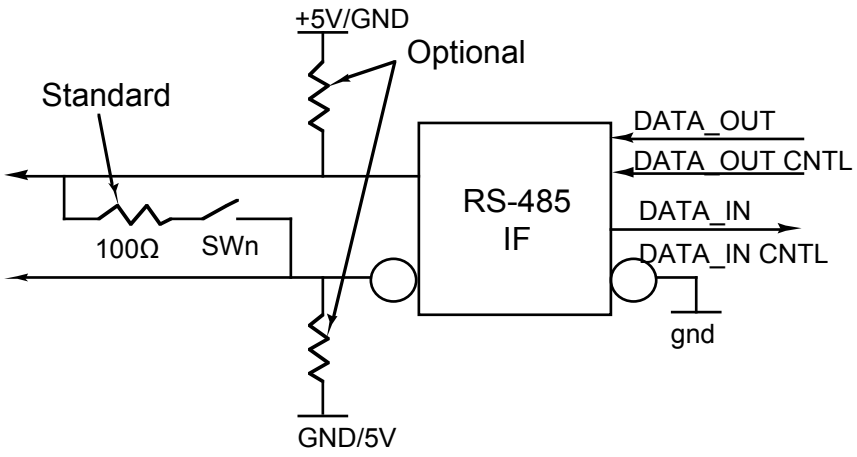

FIGURE 18 PMC-PARALLEL-485 TERMINATION

PMC-PARALLEL-485 provides for a variety of termination options. The standard termination is for programmable 100Ω parallel. Factory options include:
1) different parallel termination values
2) pull-up / pull-down resistors with either “hi” or “low” off state termination
3) Fused 3.3V reference
4) ground references
5) special circuit which receives one differential pair which is then driven out on two differential pairs and one open drain circuit.

The first two options are available on all IO pairs. The 3rd, 4th, and 5th options are restricted to certain pins. Please refer to the "Alternate" pin definitions in the next section of this document. Please contact Dynamic Engineering if an alternate configuration is needed for your project.

Loop-Back

The following signals are the interconnections made on HDEterm68 to perform loop-back testing on NG1 bezel connector.

Signal	Diff Pair		Diff Pair		Signal
Ext Clk En	1	35	8	42	IO 5
Ext Clk	2	36	7	41	IO 4
IO 3	6	40	10	44	IO 7
IO 27	30	64	34	68	IO 31
IO 26	29	63	33	67	IO 30
IO 25	28	62	32	66	IO 29
IO 24	27	61	31	65	IO 28
IO 19	22	56	26	60	IO 23
IO 18	21	55	25	59	IO 22
IO 17	20	54	24	58	IO 21
IO 16	19	53	23	57	IO 20
IO 11	14	48	18	52	IO 15
IO 10	13	47	17	51	IO 14
IO 9	12	46	16	50	IO 13
IO 8	11	45	15	49	IO 12

LEDs connected to check 3,37 = 3.3V and 4,38,5,39 = GND

PMC Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-PARALLEL-485. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 19 PMC-PARALLEL-485 PN1 INTERFACE

PMC Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-PARALLEL-485. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 20 PMC-PARALLEL-485 PN2 INTERFACE

PMC Module Front Panel IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485. Also see the User Manual for your carrier board for more information.

EXT_CLK_ENP	EXT_CLK_ENN	1	35
EXT_CLKP	EXT_CLKN	2	36
IO_0P	IO_0N	3	37
IO_1P	IO_1N	4	38
IO_2P	IO_2N	5	39
IO_3P	IO_3N	6	40
IO_4P	IO_4N	7	41
IO_5P	IO_5N	8	42
IO_6P	IO_6N	9	43
IO_7P	IO_7N	10	44
IO_8P	IO_8N	11	45
IO_9P	IO_9N	12	46
IO_10P	IO_10N	13	47
IO_11P	IO_11N	14	48
IO_12P	IO_12N	15	49
IO_13P	IO_13N	16	50
IO_14P	IO_14N	17	51
IO_15P	IO_15N	18	52
IO_16P	IO_16N	19	53
IO_17P	IO_17N	20	54
IO_18P	IO_18N	21	55
IO_19P	IO_19N	22	56
IO_20P	IO_20N	23	57
IO_21P	IO_21N	24	58
IO_22P	IO_22N	25	59
IO_23P	IO_23N	26	60
IO_24P	IO_24N	27	61
IO_25P	IO_25N	28	62
IO_26P	IO_26N	29	63
IO_27P	IO_27N	30	64
IO_28P	IO_28N	31	65
IO_29P	IO_19N	32	66
IO_30P	IO_30N	33	67
IO_31P	IO_31N	34	68

FIGURE 21 PMC-PARALLEL-485 FRONT PANEL INTERFACE STANDARD

PMC Module Backplane IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485 and routed to Pn4. Also see the User Manual for your carrier board for more information.

IO_0P	IO_0N	1	2
IO_1P	IO_1N	3	4
IO_2P	IO_2N	5	6
IO_3P	IO_3N	7	8
IO_4P	IO_4N	9	10
IO_5P-	IO_5N	11	12
IO_6P-	IO_6N	13	14
IO_7P-	IO_7N	15	16
IO_8P-	IO_8N	17	18
IO_9P-	IO_9N	19	20
IO_10P-	IO_10N	21	22
IO_11P-	IO_11N	23	24
IO_12P-	IO_12N	25	26
IO_13P-	IO_13N	27	28
IO_14P-	IO_14N	29	30
IO_15P-	IO_15N	31	32
IO_16P	IO_16N	33	34
IO_17P	IO_17N	35	36
IO_18P	IO_18N	37	38
IO_19P	IO_19N	39	40
IO_20P-	IO_20N	41	42
IO_21P-	IO_21N	43	44
IO_22P-	IO_22N	45	46
IO_23P-	IO_23N	47	48
IO_24P-	IO_24N	49	50
IO_25P	IO_25N	51	52
IO_26P	IO_26N	53	54
IO_27P	IO_27N	55	56
IO_28P	IO_28N	57	58
IO_29P-	IO_29N	59	60
IO_30P-	IO_30N	61	62
IO_31P-	IO_31N	63	64

FIGURE 22 PMC-PARALLEL-485 PN4 INTERFACE STANDARD

PMC Module Front Panel IO Alternate Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485. These are the alternate pin definitions. Also see the User Manual for your carrier board for more information.

EXT_CLK_ENP	EXT_CLK_ENN	1	35
EXT_CLKP	EXT_CLKN	2	36
3.3V	3.3V	3	37
gnd	gnd	4	38
gnd	gnd	5	39
RSTINP	RSTINN	6	40
RSTOUT1P	RSTOUT1N	7	41
RSTOUT2P	RSTOUT2N	8	42
RESET*	UNUSED	9	43
IO_7P	IO_7N	10	44
CLK1P	CLK1N	11	45
RST1P	RST1N	12	46
CLK2P	CLK2N	13	47
RST2P	RST2N	14	48
IO_12P	IO_12N	15	49
IO_13P	IO_13N	16	50
IO_14P	IO_14N	17	51
IO_15P	IO_15N	18	52
IO_16P	IO_16N	19	53
IO_17P	IO_17N	20	54
IO_18P	IO_18N	21	55
IO_19P	IO_19N	22	56
IO_20P	IO_20N	23	57
IO_21P	IO_21N	24	58
IO_22P	IO_22N	25	59
IO_23P	IO_23N	26	60
IO_24P	IO_24N	27	61
IO_25P	IO_25N	28	62
IO_26P	IO_26N	29	63
IO_27P	IO_27N	30	64
IO_28P	IO_28N	31	65
IO_29P	IO_29N	32	66
IO_30P	IO_30N	33	67
IO_31P	IO_31N	34	68

FIGURE 23 PMC-PARALLEL-485 FRONT PANEL INTERFACE ALTERNATE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC-PARALLEL-485 when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, by applying voltage less than ground or more than +5 volts with the PMC powered. With the PMC unpowered, driven input voltages should be kept within .7 volts of ground potential. The differential drivers are robust, and yet there is no sense in creating reliability issues with power sequencing and unreferenced levels.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. PMC-Parallel-485 is constructed out of 0.062 inch thick High temp FR4 material.

The PMC Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with the connectors and front panel. If more security against vibration is required the stand-offs can be secured against the carrier.

The PMC Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, taking into account the thickness and area of the PMC. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

PMC-PARALLEL-485 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
https://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois, Suite B/C
Santa Cruz, CA 95060
(831) 457-8891

support@dyneng.com

Specifications

Logic Interface:	PMC Logic Interface [PCI 33/32]
Digital Parallel IO:	32 differential IO channels. Each with direction control. Additional External Clock input and External Clock Enable.
CLK rates supported:	Multiple rate divisors supplied based on PCI, External, or board mounted oscillator.
Software Interface:	Control Registers, IO registers, IO Read-Back registers
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW aligned
Access Time:	1 PCI wait state
Interrupt:	RST1, RST2, Edge Detect
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 Pin SCSI III connector via front panel User IO routed to Pn4
Dimensions:	Standard Single PMC Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.
Temperature Coefficient:	0.89 W/^{o}C for uniform heat across PMC
Power:	Typical 300 mA @ 5V

Order Information

Temperature range components : -40⇔+85ºC

PMC-PARALLEL-485-NG1	PMC Module with 32 differential IO channels plus External clock and External Clock En. Bezel and Pn4 IO
PMC-PARALLEL-485-ENG	Engineering kit with reference software, schematic, cable and HDEterm68. [https://www.dyneng.com/HDEterm68.html]